Write VHDL code, simulate with test bench, synthesis, implement on PLD: Full adder by using half adder.

1. What are different characteristics of VHDL? Elaborate in detail.
2. Differentiate between PLA and PAL devices.
3. Explain different types of VHDL modelling style.

Half Adder-

1)

begin

**S<=a xor b;**

**C<=a and b;**

**2)**

**Begin**

**a<’0’;**

**b<’0’;**

**--hold reset state for 100 ns.**

**Wait for 100 ns;**

**a<’0’;**

**b<’1’;**

**--hold reset state for 100 ns.**

**Wait for 100 ns;**

**a<’1’;**

**b<’0’;**

**--hold reset state for 100 ns.**

**Wait for 100 ns;**

**a<’1’;**

**b<’1’;**

**--hold reset state for 100 ns.**

**Wait for 100 ns;**

**Full Adder-**

**1)**

**Begin**

**S<=(x xor y)xor z;**

**C<=((x xor y)and z) or (x and z);**

**2)**

**Begin**

**X<’0’;**

**Y=’0’;**

**Z<=’0’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’0’;**

**Y=’1’;**

**Z<=’0’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’0’;**

**Y=’0’;**

**Z<=’1’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’0’;**

**Y=’1’;**

**Z<=’1’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’1’;**

**Y=’0’;**

**Z<=’0’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’1’;**

**Y=’0’;**

**Z<=’1’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’1’;**

**Y=’1’;**

**Z<=’0’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**

**X<’1’;**

**Y=’1’;**

**Z<=’1’;**

**--hold reset state for 100 ns**

**Wait for 100 ns;**